Task #1: Digital Beamforming design and implementation

Estimated Workload: 150 hours

Estimated Delivery Date: Feb 15th, 2025

Detailed Tasks:

1- Coding the minimum variance distortionless response (MVDR) digital beamformer in C++ for two kinds of applications: Shaping of the antenna beams (in receive mode) to maximize the gain in specific directions, and Direction of Arrival (DoA) Estimation.

2- Procuring the Hardware for the Software-Defined Radio (SDR) device USRP X440 (which has an internal FPGA) and antennas.

3- Implementation and testing of the beamforming algorithm on the FPGA of the procured hardware. The testing part is to validate that the implemented algorithm is functional on the hardware platform.

Inputs:

1- Bill of Material (BOM) of the antennas and the SDR device.

2- References (book/articles) for the details of the MVDR algorithm.

3- The purpose of the use of the MVDR digital beamformer in the context of the project.

4- Any other complementary information required for the execution of this WP.

During the WP execution, recurrent follow-up meetings and discussions will be required between the candidate and the project team to ensure the WP is carried out according to the project objectives and timeline.

Expected Outcomes:

1- Fully written MVDR digital beamformer in C++ for the context of this project.

2- Implemented MVDR digital beamformer on the FPGA of the procured hardware, taking as inputs the signals from the surveillance antennas.

3- Tested implementation in real-time operation to validate that the execution of the algorithm is errorless and that the performance is acceptable in real-time.

Required profile:

- Engineering student is a minimum requirement. A Master's or bachelor's student is preferred.

- A strong RF and DSP background is a must.

- Strong coding skills in C++ and at least conversion skills from C++ to FPGA HDL are required.

- Strong troubleshooting and analytical approach.

- Engineering experience from internships in the industry is an asset.

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